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New MOSFET Package Increases Efficiency and Power Capability

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Abstract

The PolarPAK™ package (Figure 1) is a new, novel package designed to increase the power handling capability of power MOSFETs while keeping a PCB landing pattern no bigger in area than that of a standard SO-8 or PowerPAK® SO-8. Combining space savings with high-performance silicon, PolarPAK allows power supply designers to increase the power density of dc-to-dc converters without compromising performance, raising costs, or adding complexity to the manufacturing process.

INTRODUCTION

Switchmode power supply designers are constantly striving to improve the efficiency, power density, and dynamic performance of their converters. This has been facilitated by advances in silicon, using trench technology, that have lowered power MOSFET on-resistance from the tens of milliohms to less than 1 milliohm. In conjunction with these $r_{DS(on)}$ improvements, new gate structures, such as WFET®[1], have been developed to improve the switching performance of power MOSFETs without impacting the $r_{DS(on)}$ of the device. However, with surface-mount devices a remaining challenge has been finding the most efficient way to dissipate the power out of the device via the PCB and to do so without increasing the package size. An innovative new Vishay Siliconix package achieves this goal while reducing thermal resistance, package resistance, and package inductance. This in turn leads to a more efficient, faster switching power MOSFET.

A schematic of the new PolarPAK package is shown in Figure 1. As we see, the device consists of two lead frames which sandwich the silicon. In a standard package, such as a PowerPAK SO-8, only the lead frame that needs to be connected to the PCB is exposed. In the PolarPAK, both sides of the device are exposed, allowing the top of the package either to act as a heatsink or to be heatsinked. This construction enables an increase in power handling capability in forced air-cooling systems when compared to traditional MOSFET packages with an enclosed encapsulated topside lead frame. With the addition of a low-cost heatsink, placed on the top of the device, power handling is increased even further, allowing higher current levels. This is an essential capability as power requirements are increasing, especially in point-of-load dc-to-dc converters and VRMs. The industry is demanding high levels of load current within very small volume envelopes, and the PolarPAK package can handle this requirement with ease.

When housed in a package with improved junction-to-ambient thermal impedance, a power MOSFET can either handle more power or operate with a lower junction temperature. Cooler operation actually provides the most benefits in terms of efficiency and reliability. A lower junction temperature means a lower $r_{DS(on)}$, which in turn means a higher efficiency. A reduction in junction temperature of just 20 ^{o}C, can, in fact, result in a 2-½ times increase in lifetime reliability.

The paper will show the capabilities and improved efficiency of the PolarPAK package compared to conventional packages of the same size and using the same type of silicon. Using the VRM 10.1 as the platform for comparison, PolarPAK and PowerPAK SO-8 devices are investigated. The VRMs are evaluated over several load values and the efficiency is compared for the different devices.

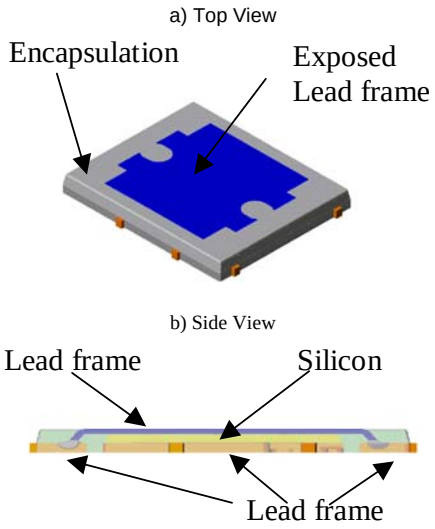

Figure 1. Schematic outline of the PolarPAK.

POLARPAK PACKAGE OUTLINE AND DESCRIPTION

Figure 2 shows a photograph of the actual PolarPAK package. The silicon die is completely encapsulated and presents the same standard footprint regardless of the specifics of the device. The top exposed part forms part of the leadframe. In other words, the size of the silicon has no impact on the landing pattern. This has several benefits. Firstly, the landing pattern is the same for any part, whether its rating is 20 V or 200 V. Secondly, the same PCB can be used for different versions of dc-to-dc converters. For example, one converter may produce a 1.5-V output, and one may produce a 5-V output. It is obvious that different silicon needs to be implemented, but the completed PCB design could stay the same. Thirdly, this consistency future-proofs the PCB layout and mechanical design against advances in silicon technology and/or cost reductions. In addition, any heatsink manufactured for the PolarPAK could be implemented on any PolarPAK device regardless of specification.

The encapsulated device also offers several advantages over an exposed die solution, including better die protection, better reliability, and easier manufacturing. It also offers the advantage of being second-sourced by other semiconductor manufacturers.

Figure 2. Photograph of the new PolarPAK MOSFET, with landing pattern

Figure 3 compares the landing patterns of the PolarPAK and the standard SO-8. With the PolarPAK layout it becomes easy to create parallel devices without compromising circuit layout and design. This allows for a lower circuit inductance. In addition, the package has a low parasitic inductance and a low profile of just 1.07 mm. As can be seen in the figure, the physical connections of the package actually take up a smaller area than that of the SO-8 package. Hence the PolarPAK allows greater power density by being able to handle more power dissipation in a smaller area.

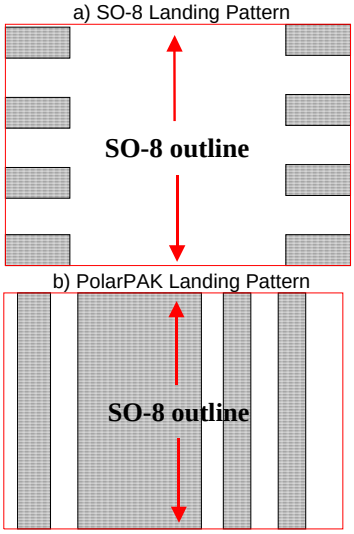

Figure 3. Comparison of landing patterns for SO-8, and PolarPAK.

THERMAL RESISTANCE ANALYSIS

A simplified thermal model of the PowerPAK SO-8 is shown in Figure 4. This shows the idealized thermal paths of the package in a two-dimensional flow. This can be equated to the circuit schematic shown in Figure 5.

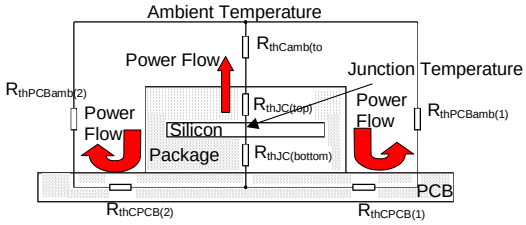

Figure 4. Simplified thermal resistance model of a Power MOSFET.

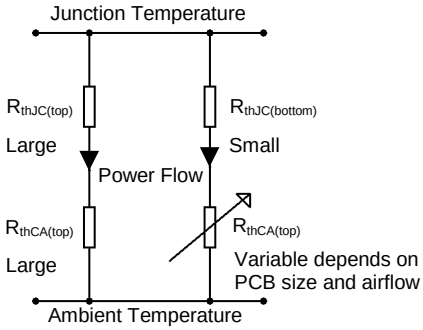

Figure 5. Equivalent circuit of PowerPAK SO-8 thermal resistance.

With the PowerPAK, the junction-to-case thermal resistance ($R_{thJC(top)}$) through the top of the package and the case-to-ambient thermal resistance ($R_{thCamb(top)}$) of the top of the package are very large, whereas the junction-to-case thermal resistance ($R_{thJC(bottom)}$) through the bottom of the package (including both the source and drain paths) is considerably lower. Also the case-to-ambient thermal resistance ($R_{thCamb(bottom)}$) of the bottom of the package, via the PCB, is considerably smaller than that seen at the top of the package.

Approaches zero
if $R_{thJA(top)}$ is large

$$\frac{1}{R_{thJA(bottom)}} + \frac{1}{R_{thJA(top)}} \cong \frac{1}{R_{thJA(bottom)}} = \frac{1}{R_{thJA(total)}} \quad [1]$$

Therefore, as Equation 1 shows, the majority of heat flow goes through the bottom of the package. The only way to increase the power capability of the device in this instance is to modify the PCB, either by increasing the landing pattern, adding extra layers, increasing the weight of the copper. or adding vias. The addition of airflow also increases the power capability, but not to a great effect.

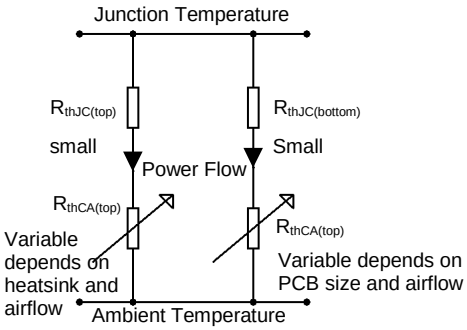

Figure 6. Equivalent circuit of PolarPAK thermal resistance.

With the PolarPAK, $R_{thJC(top)}$ is no longer considerably larger than $R_{thJC(bottom)}$ and is in fact comparable in value. The equivalent circuit schematic of the thermal paths is shown in Figure 6. If the datasheet total thermal resistances of junction to ambient are compared for the PowerPAK and PolarPAK, it can be seen that the values are approximately 25 ^{o}C/W. This is due to the fact that the values are measured without heatsinks or any forced air-cooling and are measured on a 1" by 1" FR4 PCB in still air. Therefore, even with the exposed topside of the PolarPAK, if there is no heatsink and no airflow

then the majority of the heat flow with be through the bottom of the package. Hence the bottom path dominates, and the thermal performance is similar to the PowerPAK, as shown by Equation 1. However, if a heatsink is introduced into the topside thermal path of the PolarPAK then the $R_{thCA(top)}$ thermal resistance would be greatly reduced. For example, if the heatsink had the same thermal properties as the 1"x1" PCB (24 ^{o}C/W), then $R_{thJA(bottom)}$ and $R_{thJA(top)}$ would be approximately the same (25 ^{o}C/W) and as such the total thermal resistance would be halved. In this case the PolarPAK would then have a power capability of twice that of the PowerPAK since:

$$\Delta T = P_{dissipation} R_{thja(total)} \qquad [2]$$

Insofar as the PCB is not an optimum heatsink, it is feasible that a better thermal resistance can be attained with a specifically designed heatsink and hence an even greater power capability can be achieved.

DEVICE CHARACTERISTICS

Since the PowerPAK SO-8 has become the standard for the majority of low-voltage (200-V and below) dc-to-dc converters, it is used as the point of reference for performance comparisons with the new PolarPAK.

The silicon chosen for the comparison in the PowerPAK package was the best in class, and the parameters are shown in Table 1. For the high side, a WFET device with a thick bottom oxide gate trench structure[1] was chosen, to enable fast switching performance. The low-side device chosen was a high cell density silicon structure with a very low $r_{DS(on)}$ of 3.25 mΩ.

The PolarPAK devices are shown in Table 1, and also consist of a high cell density part for the low side and a fast switching device for the high side. The Si7392DP and SiE800DF were used as the high-side (control) MOSFETs and the Si7336DP and SiE802DF were used as the low-side (synchronous) MOSFETs.

Device Number	$r_{DS(on)}$ (Ω)	Q_g (nC)	Device Technology	Package
SiE802DF	0.0023	50	High cell density (LS)	PolarPAK
SiE800DF	0.009	12	WFET (HS)	PolarPAK
Si7336DP	0.00325	36	High cell density (LS)	PowerPAK
Si7392DP	0.0115	20	WFET (HS)	PowerPAK

Table 1. Characteristics of PolarPAK device.

CIRCUIT DESCRIPTION

The test circuit used to evaluate the PolarPAK and compare the performance against the PowerPAK was a four-phase VRM 10.1 dc-to-dc converter. The controller used was an Intersil ISL6565B multi-phase controller. There was one high-side device per phase (Q1, Q3, Q5, and Q7 - Figure 4) and two low-side devices per phase (Q2, Q4, Q6, and Q8 mounted on the top of the board and Q9, Q10, Q11, and Q12 mounted on the rear of the board - Figure 4), making a total of 12 MOSFET devices on the VRM board. The layout and form factor of the VRM is shown in Figure 7. The circuit has an input voltage of 12 V, an output voltage of 1.3 V, and a switching frequency of 450 kHz.

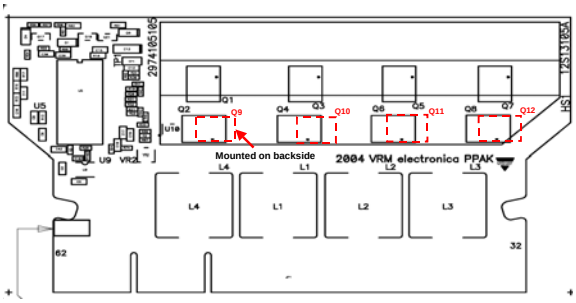

Figure 7. Outline of the four-phase 10.1 VRM

EXPERIMENTAL RESULTS

The VRM was tested using a regenerative load module developed by PEI Technologies[2]. Figure 8 shows the test setup including the VRMs, regeneration load modules, wind tunnels, and ac/dc power supply. This allowed the converters to be tested with a load current up to 80 A and an airflow rate of up to 600 LFM.

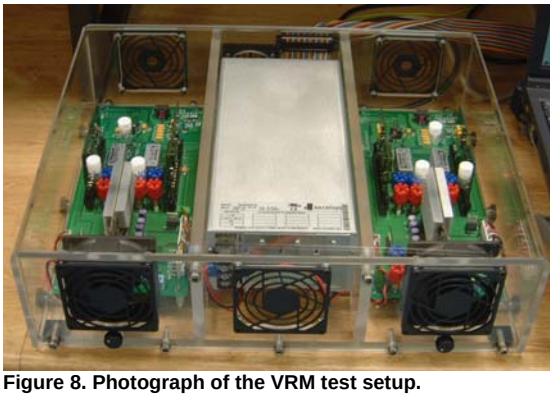

Figure 8. Photograph of the VRM test setup.

Figure 9 shows the efficiency measurements, across the load range, for both the PolarPAK and PowerPAK, with an airflow rate of 400 LFM. At low loads the increase in efficiency of the PolarPAK VRM is negligible, but at higher loads the increase is more dramatic. For example, at 80 A (20 A per phase) the efficiency increase by using the PolarPAK is 6 %, whereas at 20 A (5 A per phase) it is just 0.4 %. It is envisaged that at higher current levels the efficiency gain will be even greater.

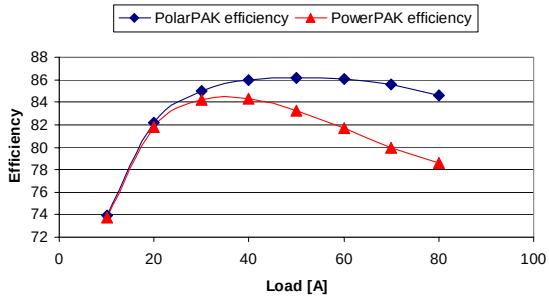

Figure 8. Efficiency results for the PolarPAK vs PowerPAK with an Airflow of 400LFM, Vin 12 V and Vout 1.3 V.

Figure 9 shows the temperature measurements, taken close to the source connection of the devices on the PCB. Although this is not an absolute measurement of the junction temperature, it is representative of the junction temperature. Again it can be seen that at low loads (<40 A total, 10 A per phase) the improvement in junction temperature of the PolarPAK is negligible, but at the higher load currents above 60 A (or 15 A per phase) the temperature improvement is very significant. With an 80-A load current (20 A per phase), the temperature improvement with the PolarPAK is over 30 ^{o}C.

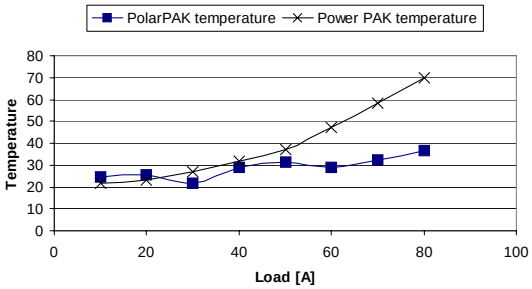

Figure 8. Temperature results for the PolarPAK vs PowerPAK with an Airflow of 400LFM, Vin 12 V and Vout 1.3 V.

CONCLUSIONS

The new MOSFET package presented in this paper has the ability to dissipate power both through the bottom of the package into the PCB, and through the top of the package into ambient. It has been shown that this ability is greatly enhanced when used with a forced air cooling system and will be improved even further with the addition of a top side heatsink. No longer is the package limited by the constraints of the PCB, but it is now free to dissipate greater power, all within the same space envelope. It has also been shown that the efficiency of the converter is greatly improved by using this package (6% at an 80-A load) and also that the junction temperature is reduced, which improves the reliability of the dc-to-dc converter.

Since the package encapsulates the silicon, it has several advantages over exposed-die solutions, including better reliability and a consistent PCB footprint. But it also retains certain advantages of a exposed die solution, such as a low parasitic package inductance and low circuit inductance. With all the factors taken into account this package will allow the dc-to-dc converter designer to increase power density by the addition of airflow or heatsinks, but without compromising performance or adding complexity to the manufacturing process.

REFERENCES

1 Jess Brown 'Modeling The Benefits of Using a Thick Bottom Oxide Gated MOSFET (WFET®) With Increased Switching Performance in the High Side of a Non-Isolated Buck Converter.', APEC 2004, California, USA

2 B. O'Sullivan, R. Morrison, M.G. Egan, J. Slowey, B. Barry 'A regenerative load system for the test of Intel VRM 9.1 compliant modules', APEC 2004, California, USA.